Market Update

Peter Jenkins
Vice President, Marketing

24 November 2014

INVESTOR DAY
ASMLSMALLTALK2014
LONDON

Forward looking statements

This document contains statements relating to certain projections and business trends that are forward-looking, including statements with respect to our outlook, expected customer demand in specified market segments, expected sales levels and trends, our market share, customer orders and systems backlog, IC unit demand, expected or indicative financial results or targets, including revenue, gross margin, expenses, gross margin percentage, opex percentage of sales, tax percentage, cash conversion cycle, capex percentage of sales, credit rating and earnings per share, expected shipments of tools and the timing thereof, including expected shipments of EUV and DUV tools, productivity of our tools and systems performance, including EUV system performance (such as endurance tests), the development of EUV technology and timing of shipments, development in IC technology, including shrink scenarios, NAND technology development and cost estimates, expectations on development of the shrink roadmap across all of our systems, upgradeability of our tools, system orders, customer transition estimates, expected transition scaling, forecasted industry developments, including expected smartphone, tablet and server use in future years, and expectations relating to new applications including wearable devices and connected devices, expected investment pay-back time for foundries, expected construction of additional holistic lithography infrastructure, the continuation of Moore's Law, and our dividend policy and intention to repurchase shares. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them.

Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors (the principal product of our customer base), the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, affordability of shrink, the continuation of Moore's Law, the impact of manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of new products and customers meeting their own development roadmaps, market demand for our existing products and for new products and our ability to maintain or increase or market share, the development of and customer demand for multi-patterning technology and our ability to meet overlay and patterning requirements, the number and timing of EUV systems expected to be shipped, our ability to enforce patents and protect intellectual property rights, the risk of intellectual property litigation, EUV system performance and customer acceptance, availability of raw materials and critical manufacturing equipment, trade environment, our ability to reduce costs, changes in exchange rates and tax rates, available cash, distributable reserves for dividend payments and share repurchases, changes in our treasury policy, including our dividend and repurchase policy, completion of sales orders, the risk that key assumptions underlying financial targets prove inaccurate, including assumptions relating to market share, lithography market growth and our customers' ability to reduce productions costs, risks associated with Cymer, which we acquired in 2013, and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

Outline

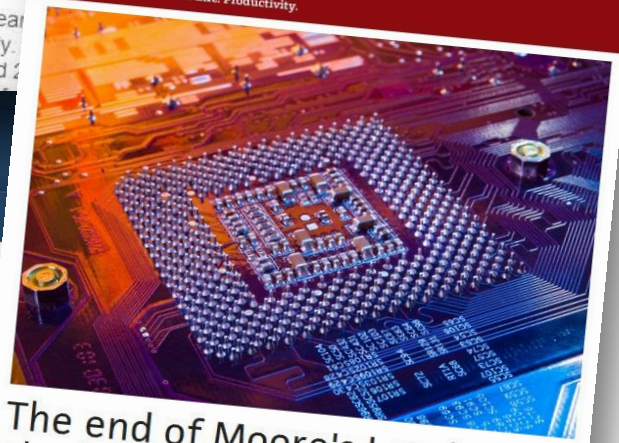
- **Introduction**
- ASML value drivers
- Market opportunity & affordability

Some people are predicting the imminent end of Moore's law

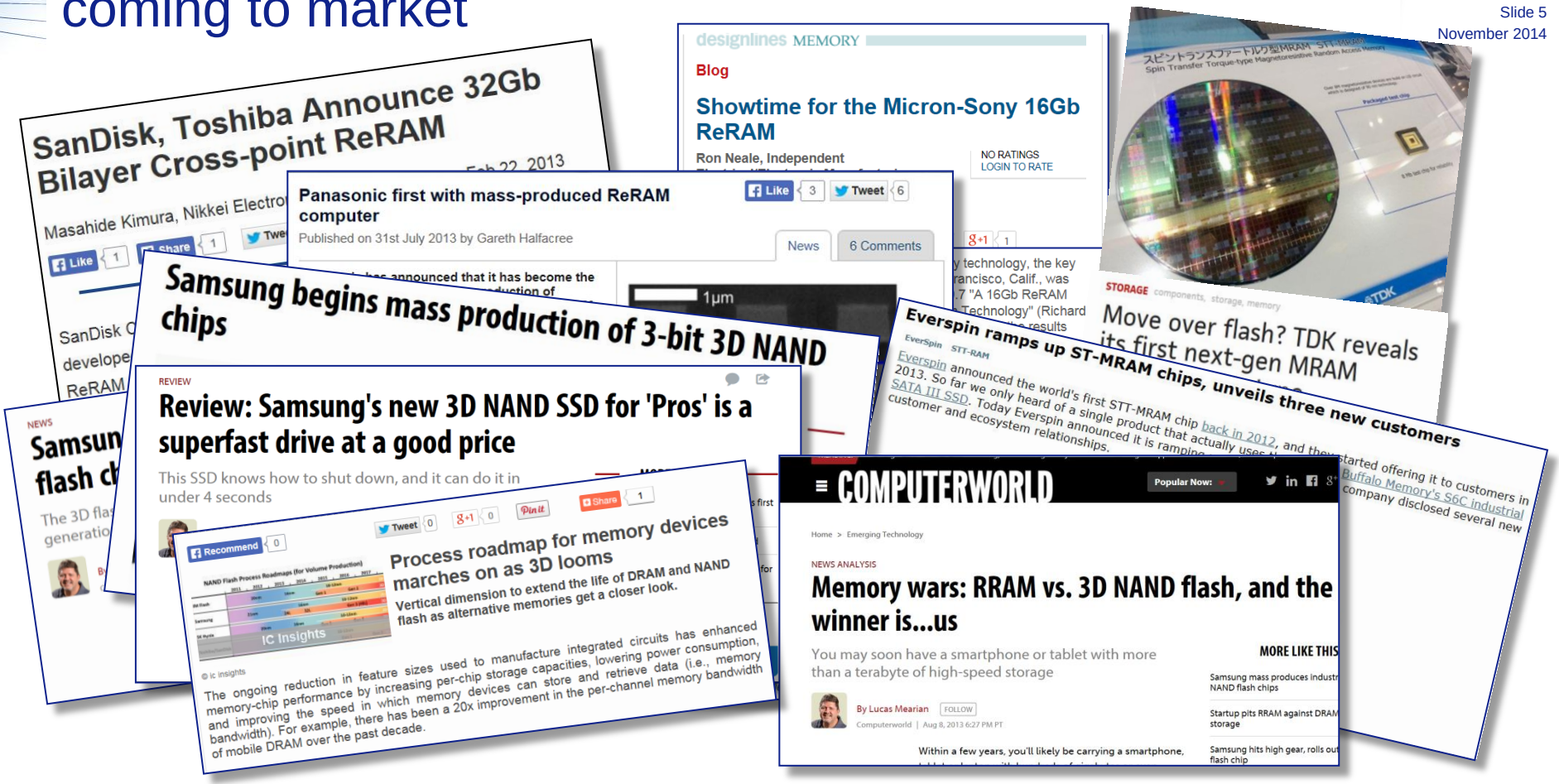
c|net
Search CNET
End of Moore's Law: It's not just about physics
A DARPA direc
why you now
insurmountab
by Brooke Crothers

EE Times
28nm – The Last Node of Moore's Law
Zvi Or-Bach, Mon
3/19/2014 06:46 PM E
We have been hear
quite a lot recently.
the 7nm node and 2
recognize that

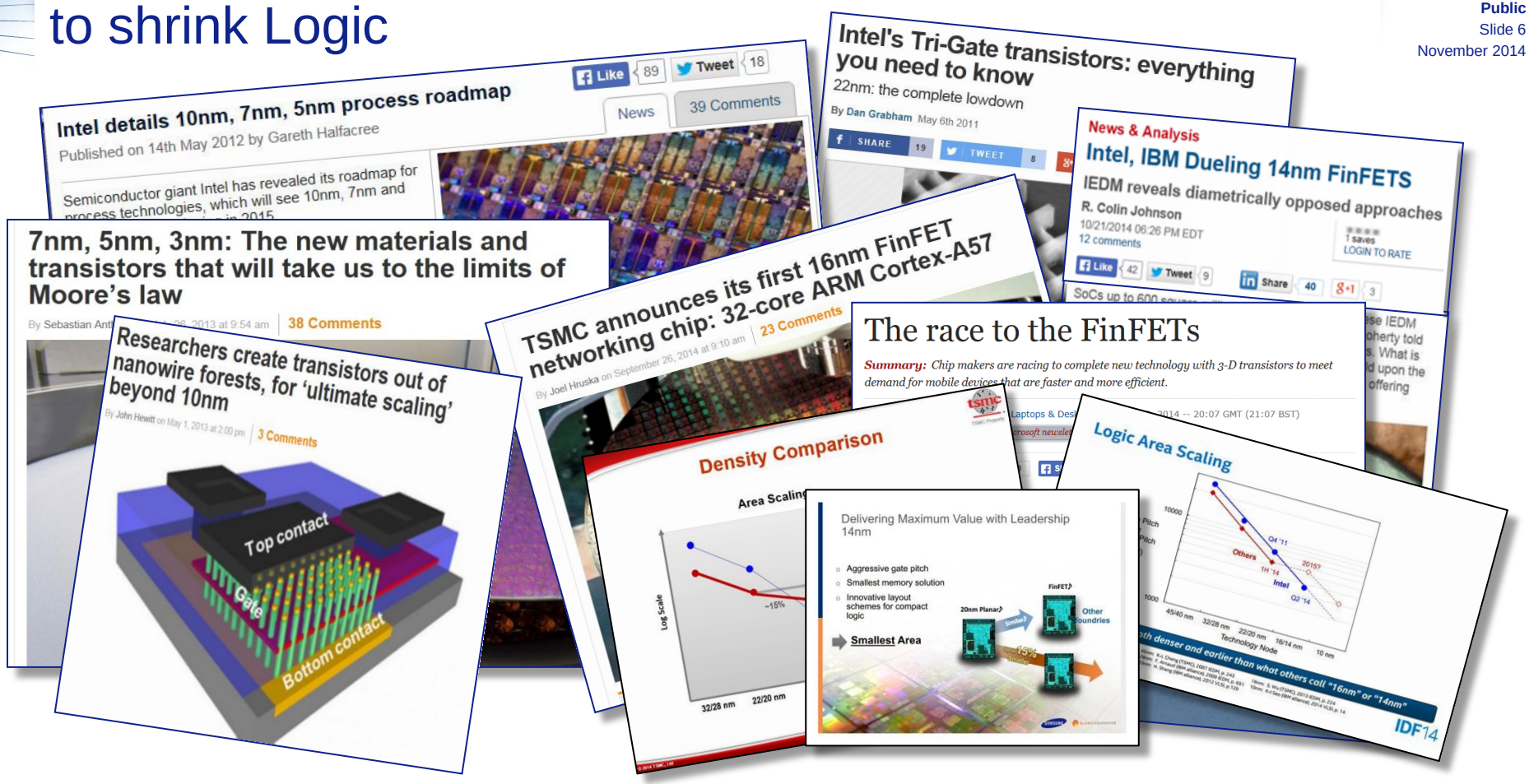
ZDNet
Hot Topics Reviews Downloads Newsletters White Papers
Moore's Law: the end is near-ish!
By Gery Menegaz for Five Nines: The Next Gen Datacenter | July 16, 2012 -- 22:59 GMT (23:59 BS
Many agree that one of the key driving forces of the computer revolution is the ability to
provide consumers with devices of ever increasing power. Every year manufacturers put o
a new line of more powerful products – twice as powerful, in fact, every 18 months. And,
we can believe Michio Kaku, in his book the Physics of the Future, this is about to come t
an end.

PCWorld
Work. Life. Productivity.

The end of Moore's Law is on the horizon, says AMD
Ian Paul
@ianpaul
Apr 3, 2013 9:55 AM

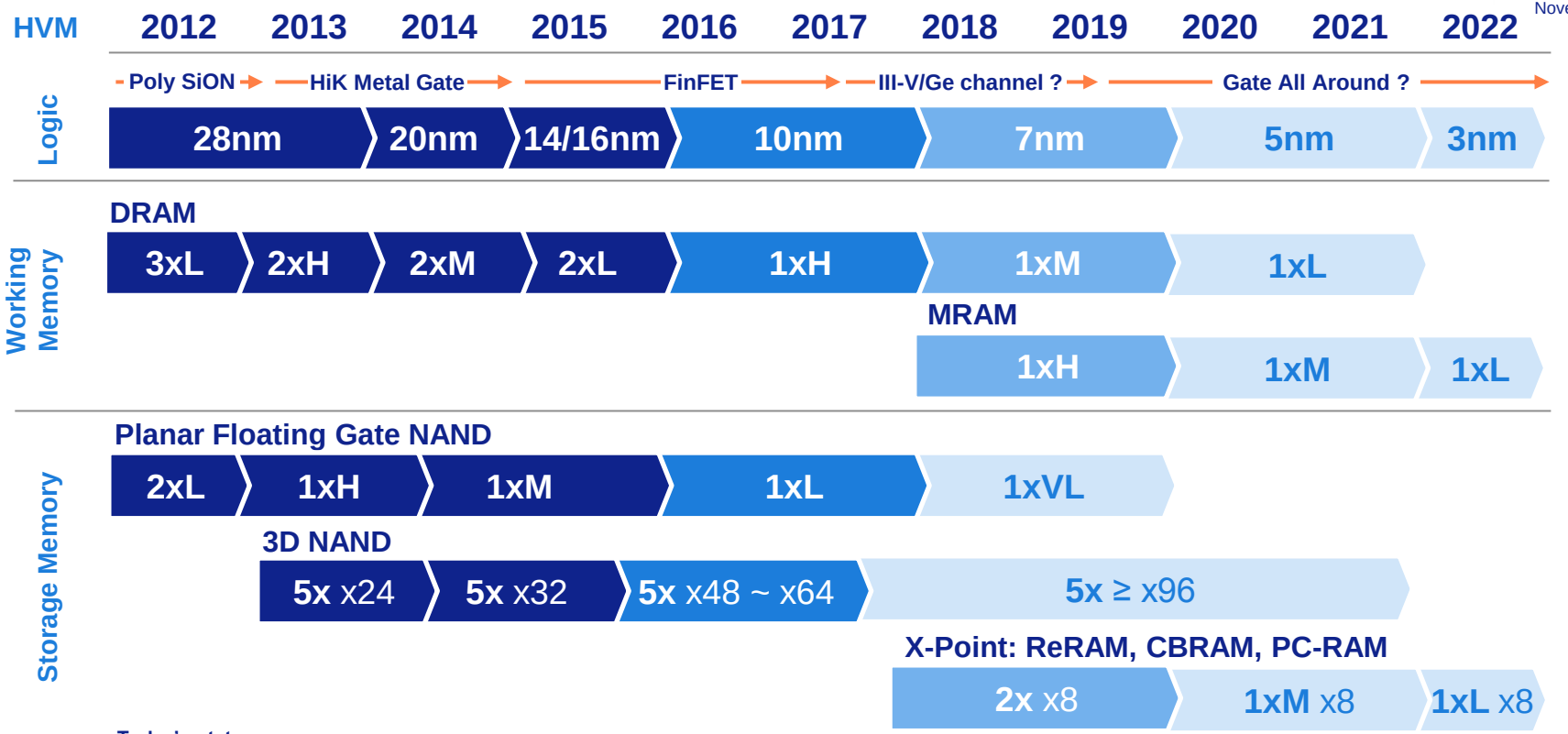
There is a rich pipeline of new scalable memory devices coming to market



and plenty of ideas & competition on how to continue to shrink Logic



Customer Shrink Roadmap



Source: ASML, Customer roadmaps

Process evolution essential to enable increasing processing & graphics capabilities of mobile devices

Shrink : Integrate functions, increase processor & memory capacity, improve speed & power efficiency, lower cost

Add functions, increase die size, cost

65nm	45nm	32nm	28nm	22nm	20nm	14nm
A2298 72mm²	A4 53mm²	Core i7-990 240mm2	A6 97mm²	A7 102mm²	Core i7-4960 257mm2	A8 90mm²	Core M 82mm²
Core2 E4700 111mm2	A5 122mm²	Exynos 3 118mm²	A6X 123mm²	S600 88mm²	Exynos 5 122mm²	A8x 128mm²	Exynos 7420
Core2 Q6700 286mm2	A5X 169mm²	Core i7-920 263mm²	Core i7-3960 435mm2	S800 118mm²	Exynos 5420	Core i7-5960 355mm2	S810	

Axx : Apple. Sxx : Qualcomm Snapdragon. Core2, Core i7 and Core M : Intel

Sources: ChiipWorks, Intel, Samsung, Qualcomm, Apple

Process evolution essential to enable increasing processing & graphics capabilities of mobile devices

Shrink : Integrate functions, increase processor & memory capacity, improve speed & power efficiency, lower cost

Add functions, increase die size, cost

65nm

2009
iPhone 3G

45nm

2010
iPhone 4
iPad

2011
iPhone 4S
iPad 2

2011
Galaxy S2

2012
iPad 3

32nm

2012
iPhone 5
iPad 3

Cobra PC

2012
iPad 4

28nm

2013
iPhone 5S
iPad Air

HTC 1

2013
Galaxy S4

Lenovo
Vibe

Chrome-
book 2

22nm

Touchscreen Laptop

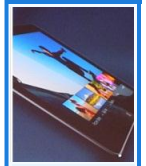
20nm

2014
iPhone
6/6+

2014
iPad Air 2

Xperia Z4

14nm



2015
in mobile
products

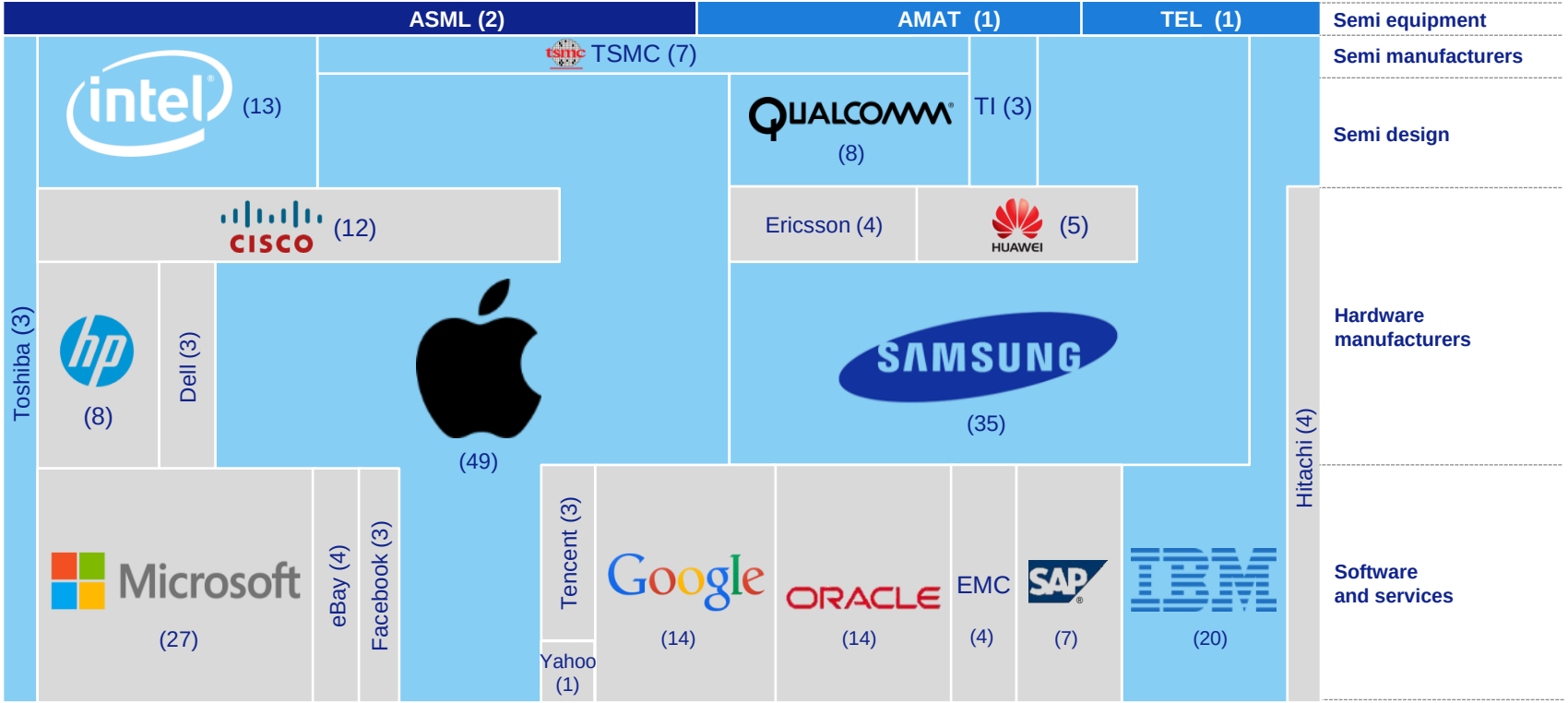
Products : Add functions e.g. cameras , increase screen & video resolution, improve data speed & battery lifetime

Axx : Apple. Sxx : Qualcomm Snapdragon. Core2, Core i7 and Core M : Intel

Sources: ChiipWorks, Intel, Samsung, Qualcomm, Apple

Enabling an ecosystem that has considerable financial means and strong incentives to drive innovation …

Leading technology companies in the semiconductor industry ecosystem (EBIT 2013, B$)



Outline

- Introduction
- **ASML value drivers**
- Market opportunity & affordability

EUV Value Driver : 3 ~ 5x Resolution Enhancement

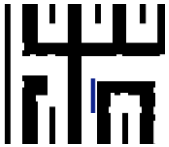
ArF immersion

k_1
difficulty,
limit = 0.25

k_1 = 0.265
strong OPC mask

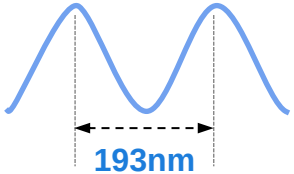
EUV

Resolution = $k_1 \times \frac{\lambda}{NA}$

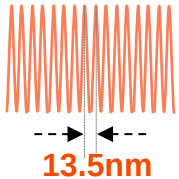


k_1 = 0.32
OPC mask

λ
Wavelength



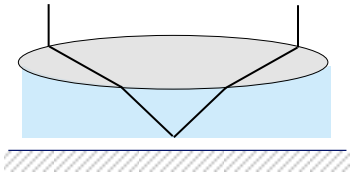
193nm



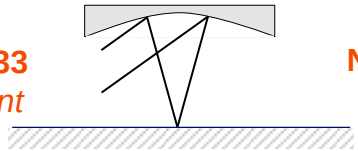
13.5nm

NA
Numerical
Aperture

NA 1.35
Maximum



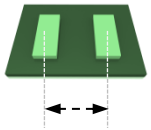
NA 0.33
Current



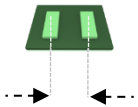
NA > 0.5
Future

Resolution
Minimum pitch

76nm
38nm half pitch



26nm
13nm half pitch



< 16nm
< 8nm half pitch

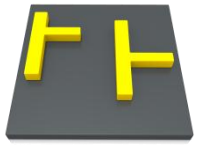
There are multiple roads to shrink

Process Flow

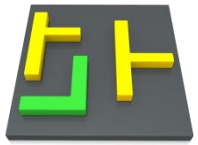
2D Multi Patterning or EUV single expose

LELE (or EUV SE)

LE #1



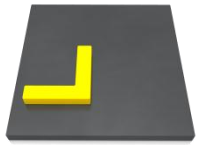
LE #2



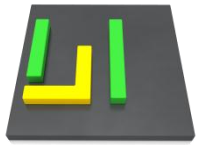
- Suitable for 1D or 2D patterning
- Overlay control of each layer is a key

LELELE (or EUV SE)

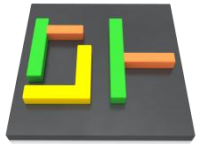
LE #1



LE #2



LE #3



1D Self Aligned Multiple Patterning (SAMP)

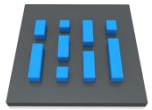
SADP (D=Double)

Mandrel

Spacer

Spacer cut

Patterning cut(s)

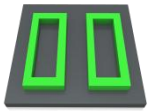


- Suitable for 1D layout. (← better CD, LWR control)
- May need multiple cut patterns

SAQP (Q=Quadruple)

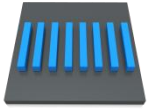
Mandrel

Spacer #1

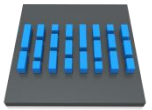


Spacer #2

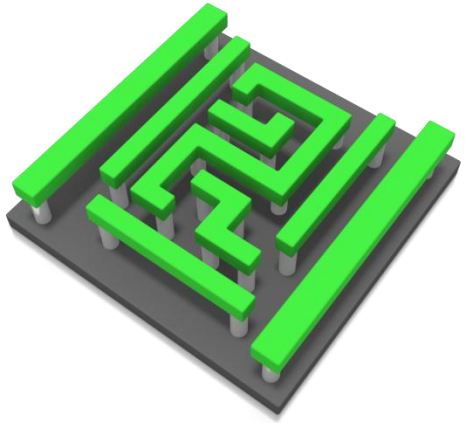
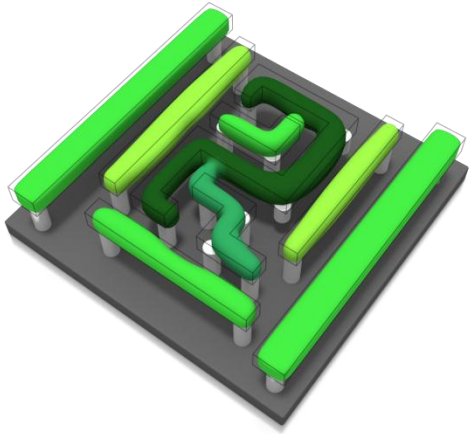
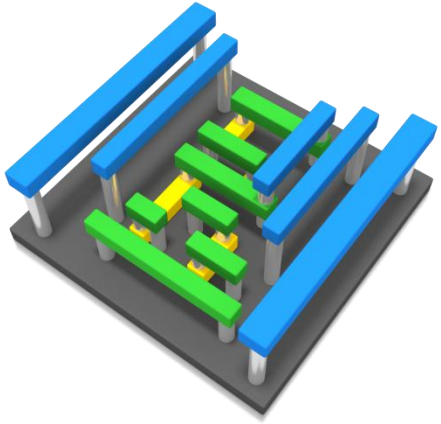
Spacer cut



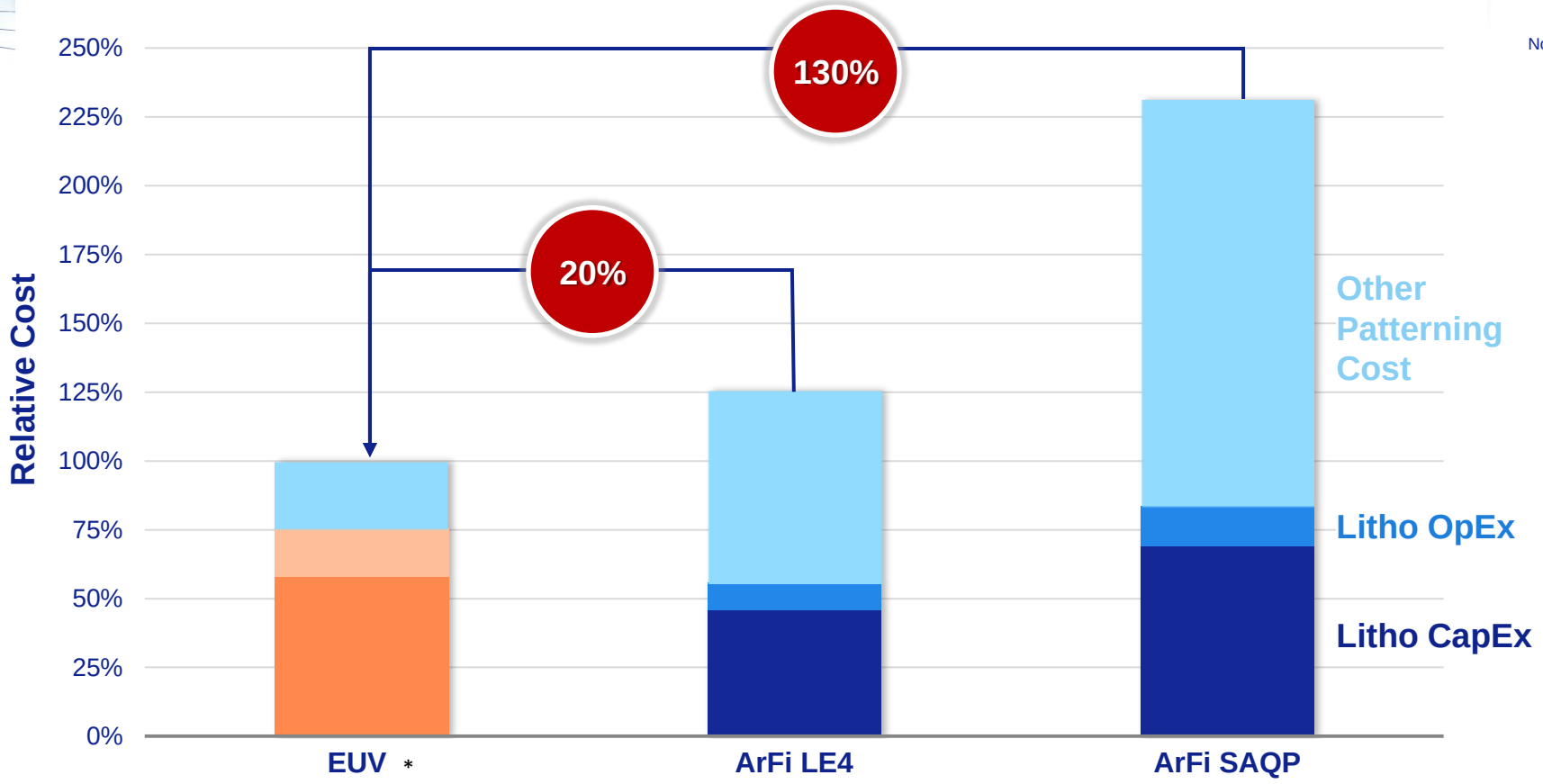
Patterning cut(s)



EUV process simplification example :
2D Logic Metal Interconnect illustration

EUV Single patterning	ArFi LE^4 Patterning	ArFi SAQP
		
# Steps		
Mask 1	**Mask** 4	**Mask** 6
Etch 1	**Etch** 4	**Etch** 9
Spacer	**Spacer**	**Spacer** 4

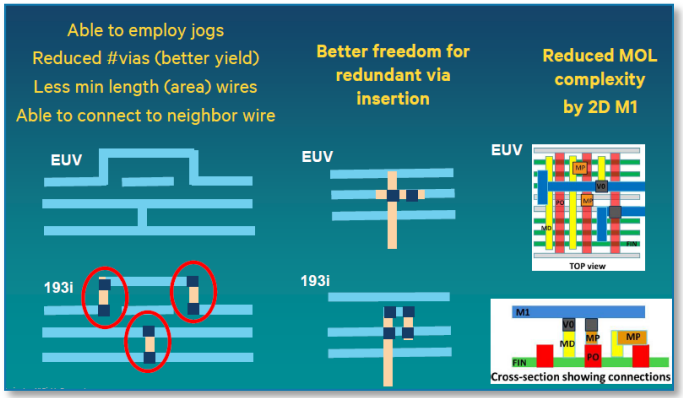
EUV Processing Cost per Layer saving: 20% ~ 130%

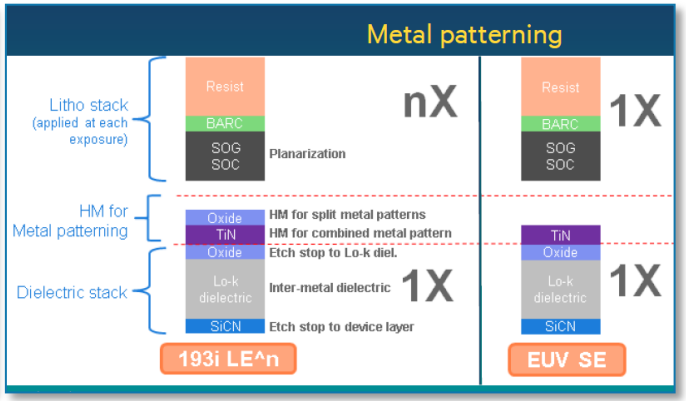


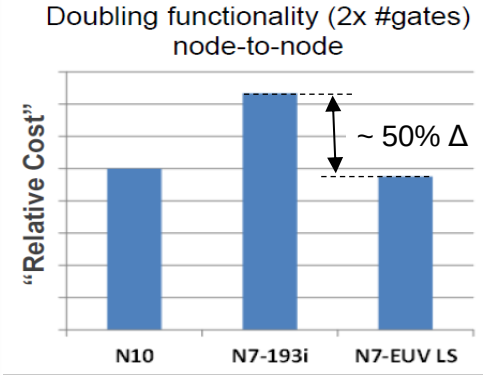
* NXE:3350B, 95WPH, 30mJcm^{-2}

EUV Resolution Benefits > Patterning Cost Reduction

1 2D Patterning + 2 Process Simplification = 3 Lower Cost Shrink







More effective shrink
- Smaller die due to reduced design constraints
- More die per wafer
- Higher yield

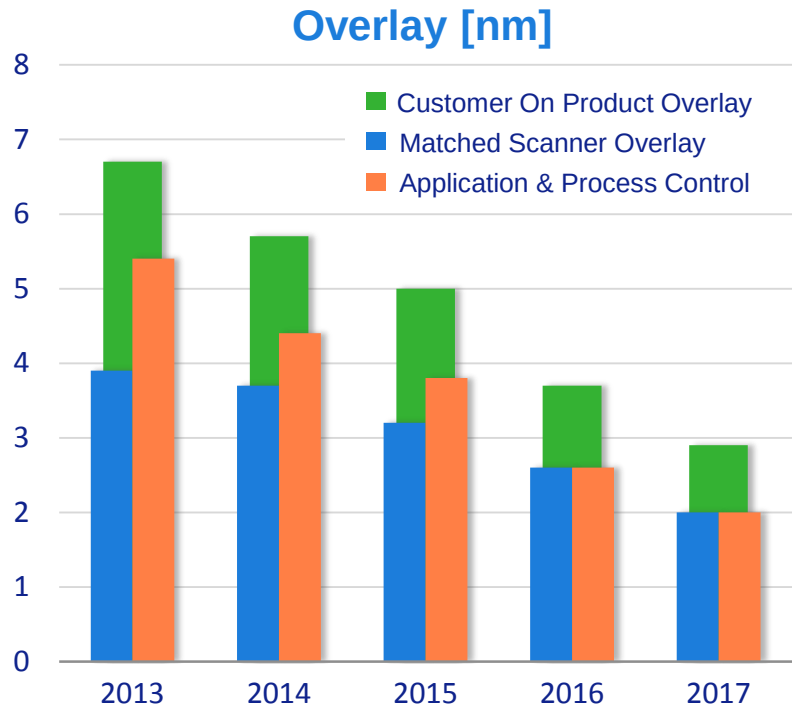
Fewer process steps
- Higher defect limited yield
- Faster cycle times

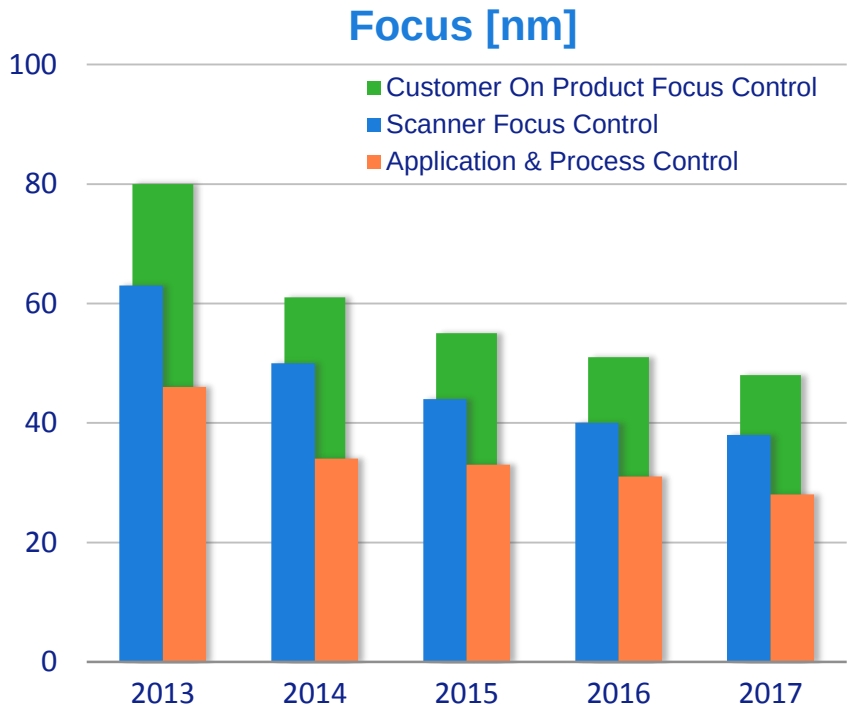
- Lower patterning cost
- Fewer process steps
- More effective shrink
- Higher yield

Reference: Esin Terzioglu, Qualcomm, 2014 International Symposium on EUV, October 27, 2014

Customer roadmaps require continuous improvement in Lithography Overlay and Focus Performance

ASML holistic roadmap delivers both scanner & process application improvements to secure low rework & high yield in volume manufacturing





Overlay Value: 1nm improvement @ 20nm Logic Node ~ €100M Cost Saving per Year for 100k WSpM

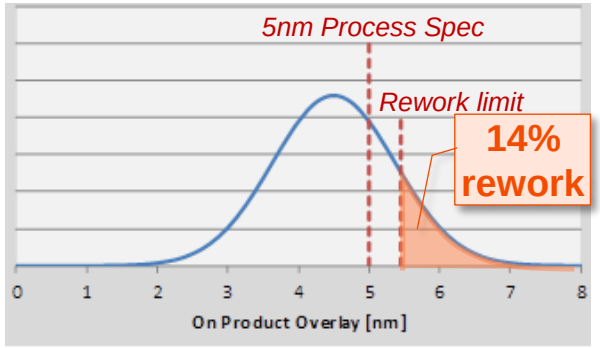
6nm Overlay

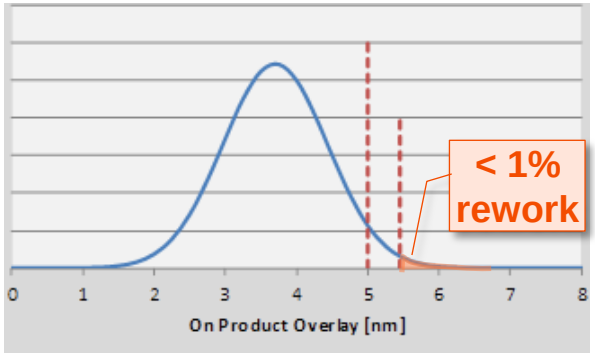
5nm Overlay

Production Cost Saving

Lot-Lot Statistical Overlay Process Control

13% Rework
~ €33M / year



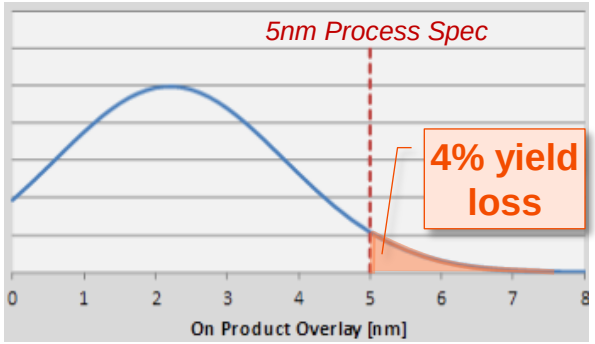


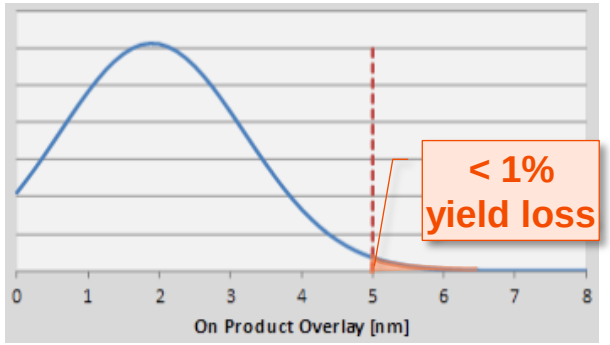
ArFi Rework Cost : ~ €15 / wafer, 100,000 wafers / month, 14 overlay critical immersion exposure passes

Die Yield Cost Saving

Statistical Overlay Die Yield

3% Die Yield
~ €67M / year

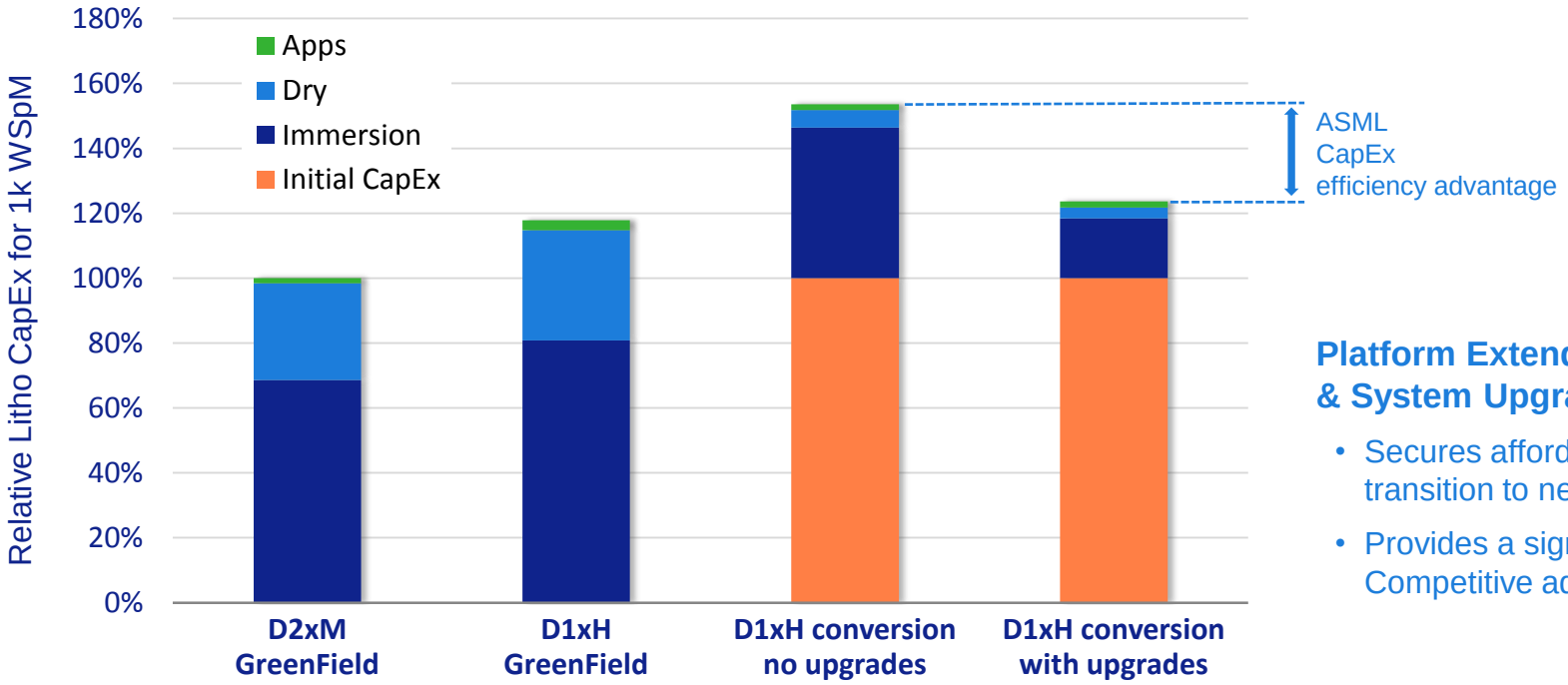




Die cost : ~ €3.70, 100,000 wafers / month, Die size = 100mm^2, ~ 630 die / wafer

ASML Platform approach enabling Extendibility & Upgradability has been an essential factor in ASML success in the Memory sector

Example : DRAM process migration from D2xM to D1xH



Platform Extendibility & System Upgrades

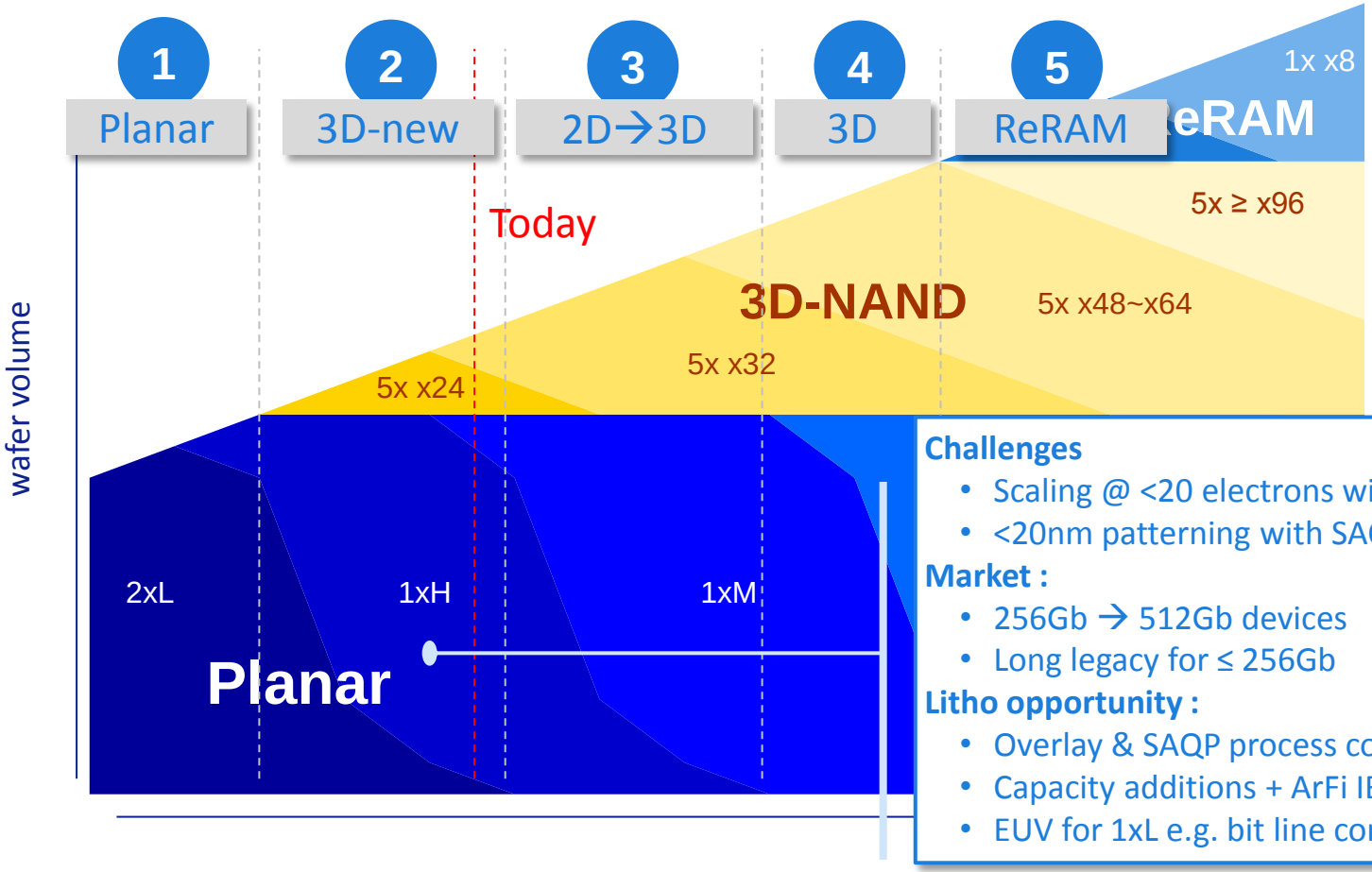
- Secures affordability of transition to next node
- Provides a significant Competitive advantage

D2xM : 18 immersion layers, 30 dry layers, 6nm On-Product Overlay
D1xH: : 21 immersion layers, 35 dry layers, 4nm On-Product-Overlay, 50% immersion layers critical overlay

Outline

- Introduction
- ASML value drivers
- **Market opportunity & affordability**

NVM market transitions & ASML opportunities



Challenges

- Scaling @ <20 electrons with 3-bit/cell
- <20nm patterning with SAQP

Market :

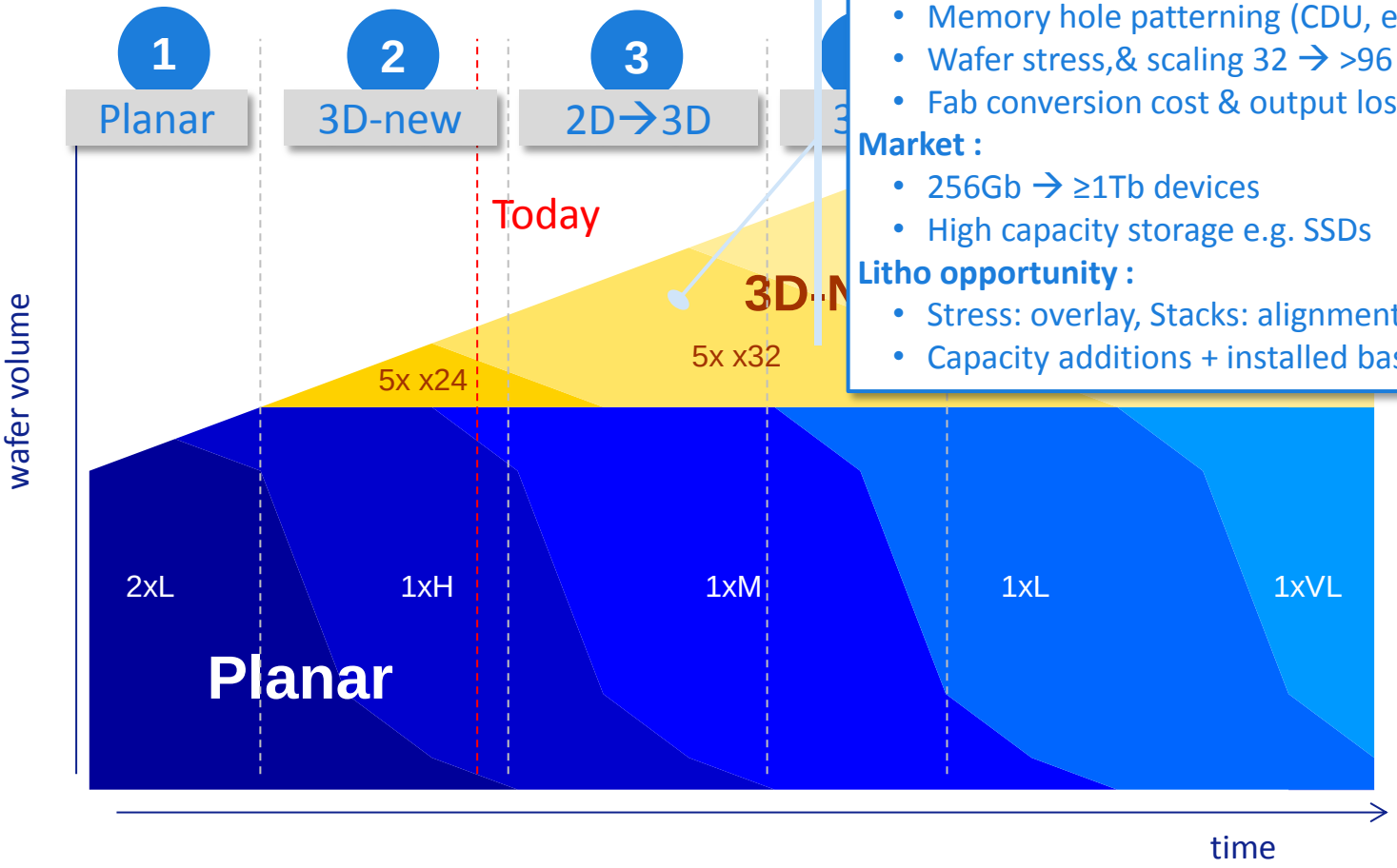
- 256Gb → 512Gb devices
- Long legacy for ≤ 256Gb

Litho opportunity :

- Overlay & SAQP process control for ≤1xM
- Capacity additions + ArFi IB upgrades
- EUV for 1xL e.g. bit line contact

NVM market transitions & ASML opportunities

ASML



Challenges :

- Memory hole patterning (CDU, elipticity, slope)
- Wafer stress,& scaling 32 → >96 stacks
- Fab conversion cost & output loss → new fabs

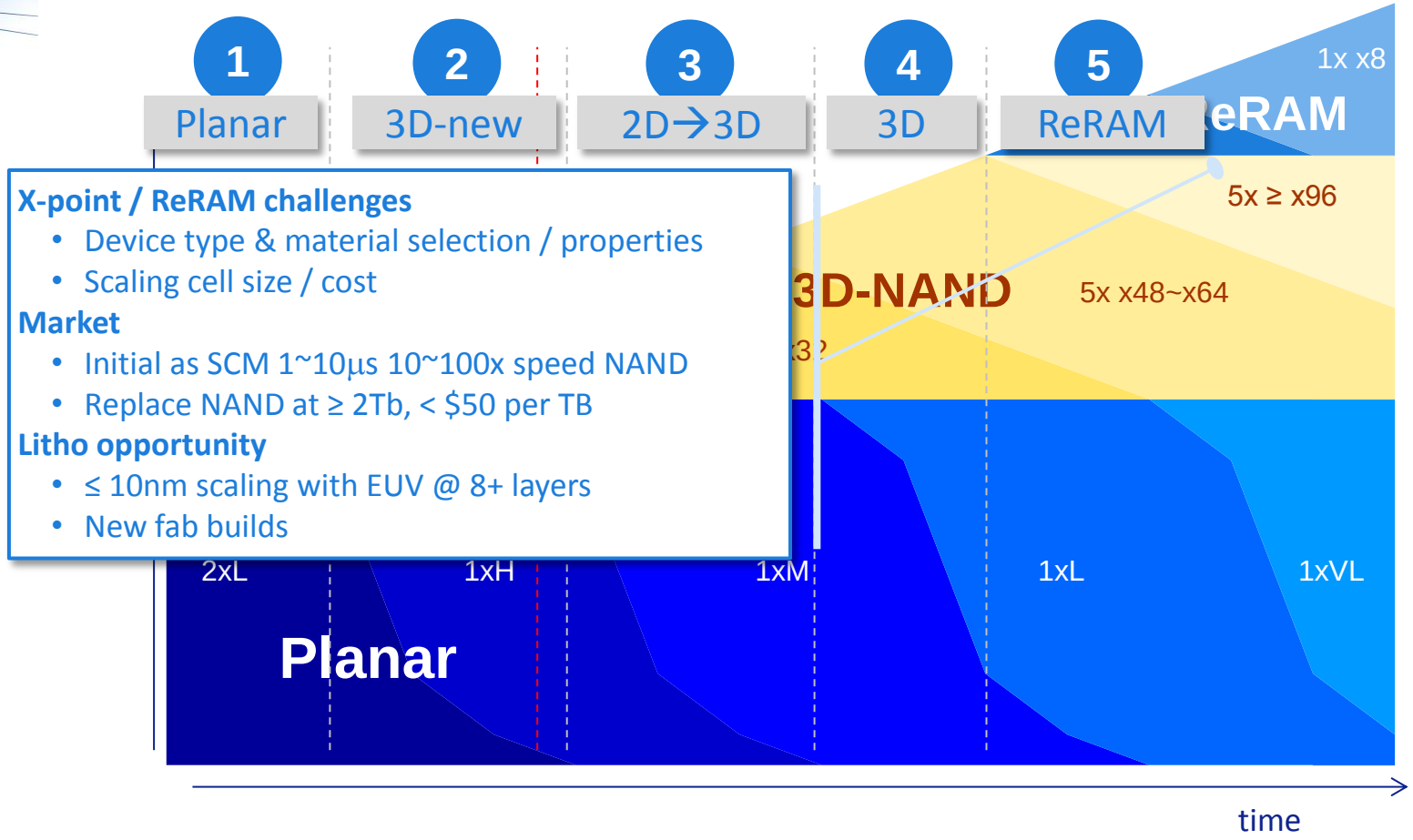
Market :

- 256Gb → ≥1Tb devices
- High capacity storage e.g. SSDs

Litho opportunity :

- Stress: overlay, Stacks: alignment & focus
- Capacity additions + installed base upgrades

NVM market transitions & ASML opportunities



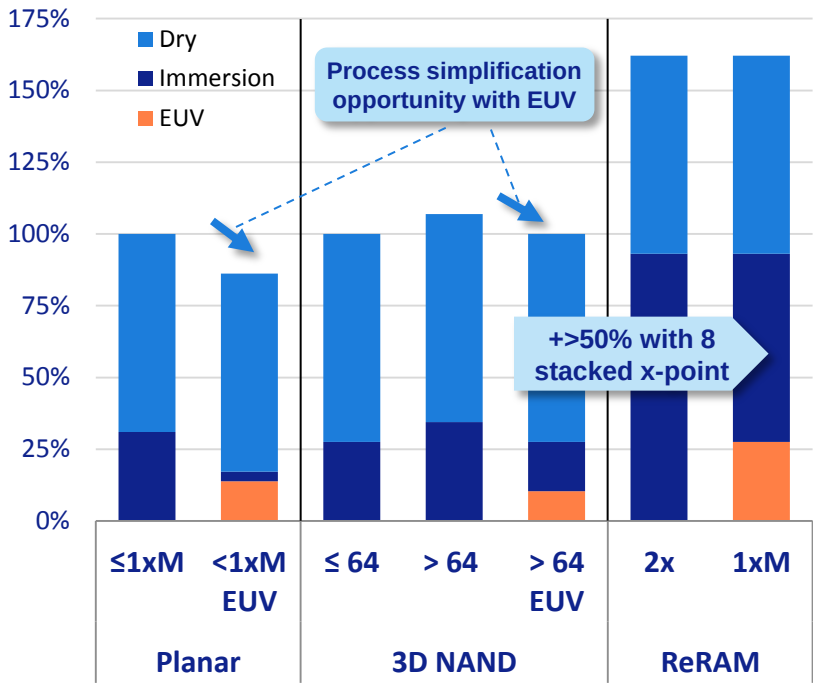
X-point / ReRAM challenges
- Device type & material selection / properties
- Scaling cell size / cost

Market
- Initial as SCM 1~10µs 10~100x speed NAND
- Replace NAND at ≥ 2Tb, < $50 per TB

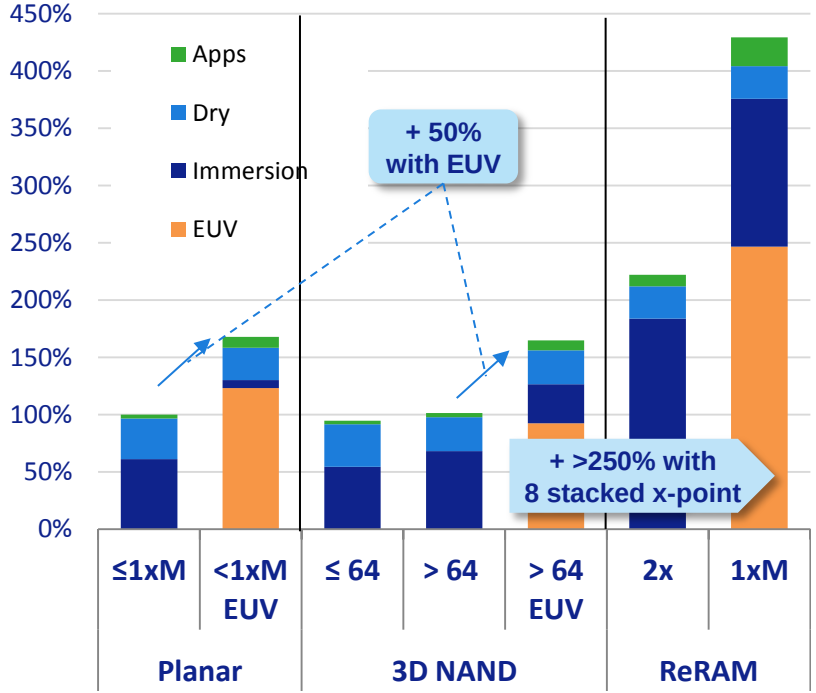
Litho opportunity
- ≤ 10nm scaling with EUV @ 8+ layers
- New fab builds

Lithography market opportunity for Flash Memory EUV insertion for scaling Planar & 3D, ReRAM

Relative Exposure Passes

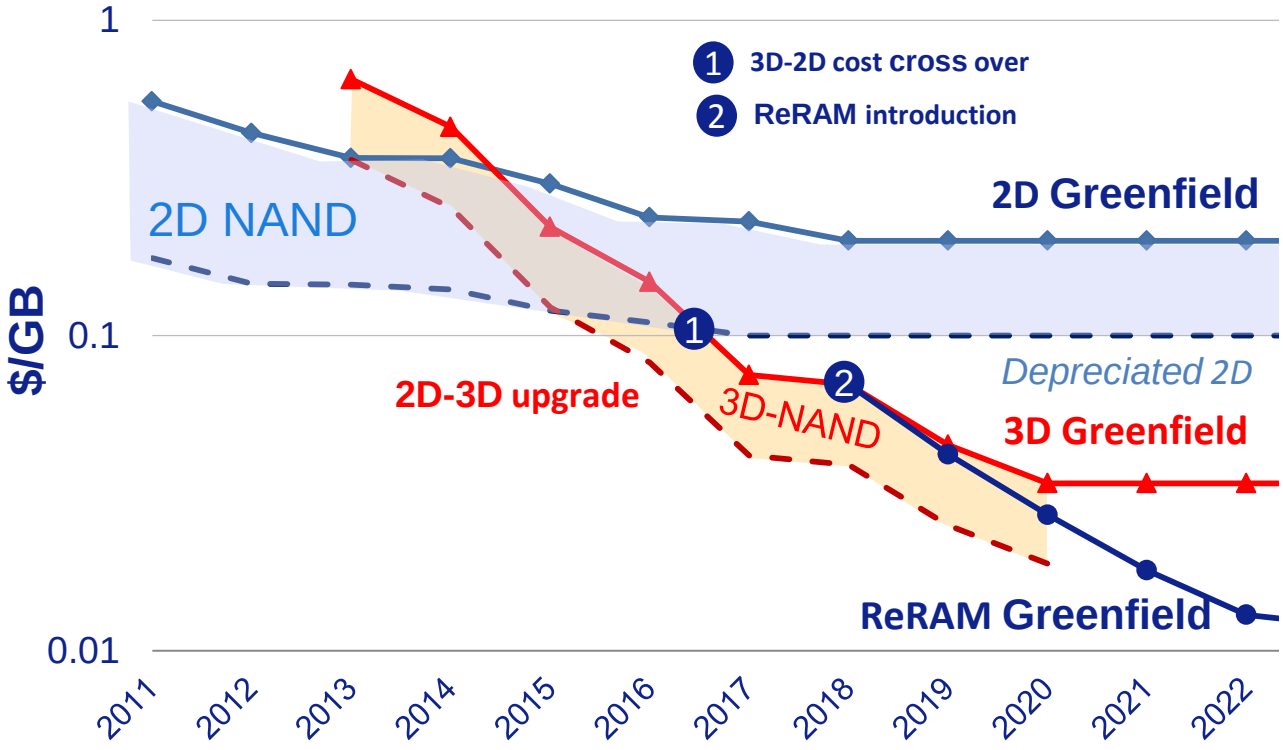


Relative CapEx / 1k WSpM



Source: ASML

NAND bit cost scaling and customer transition estimates



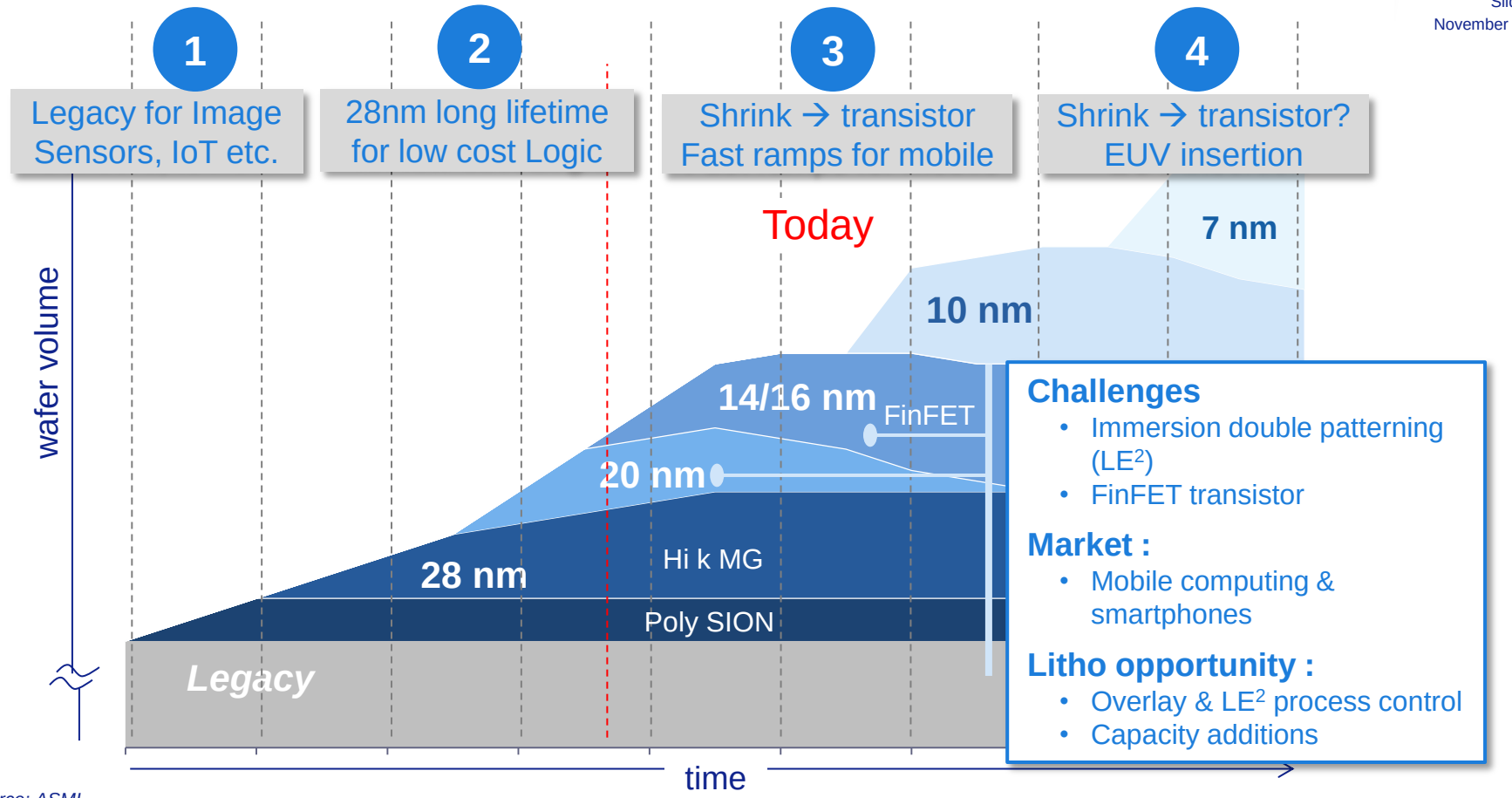
3D NAND transition challenges

- Capital expenditure to convert a fab from planar to 3D ~ 4x normal planar node conversion
- >40% reduction in max fab wafer starts capacity
- Lost wafer start output due to conversion downtime

Conclusion: 3D capacity will be largely Greenfield

Source: ASML, IC Knowledge, Forward Insights

Logic market transitions & ASML opportunities



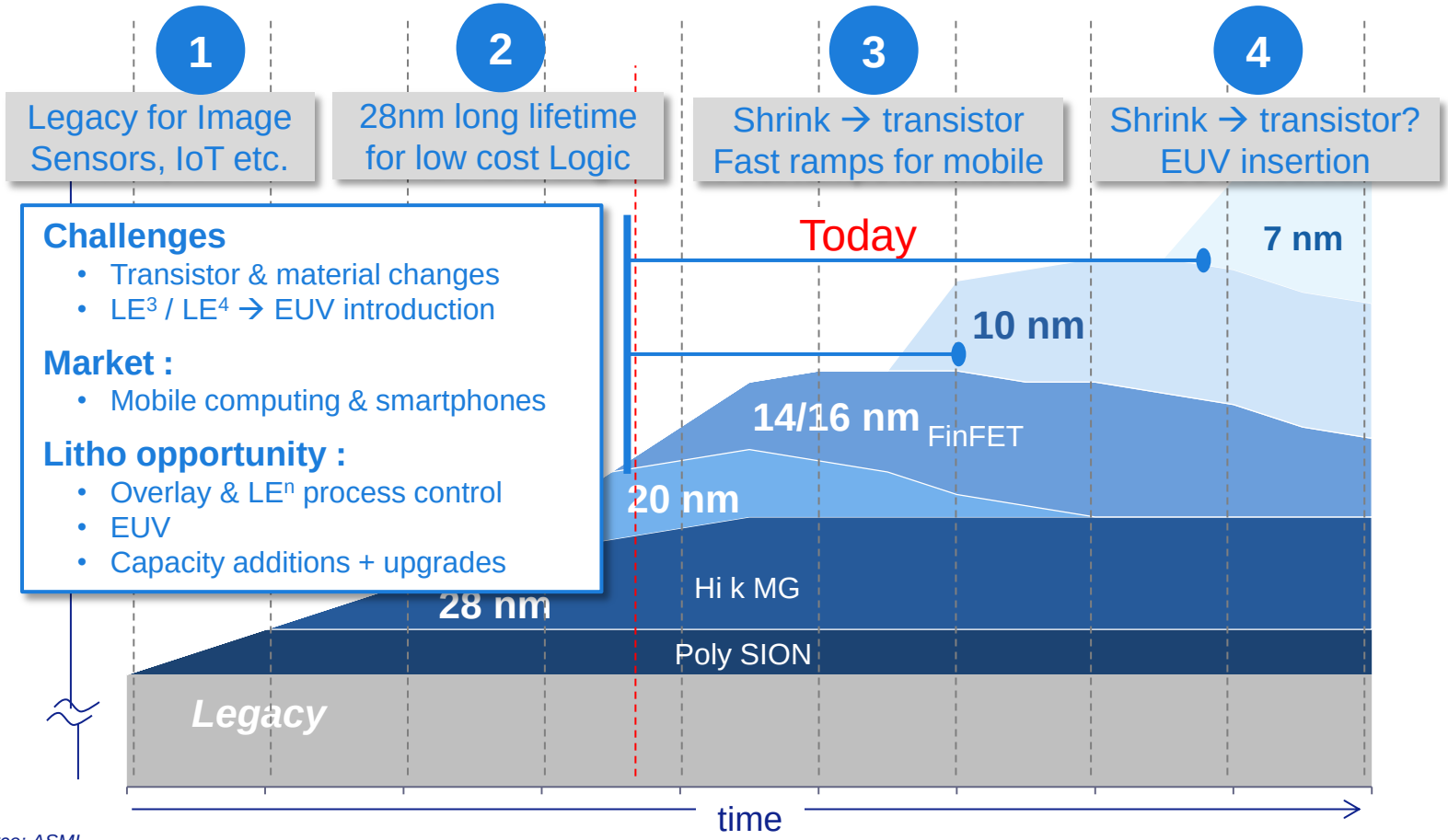
Challenges
- Immersion double patterning (LE^2)
- FinFET transistor

Market :
- Mobile computing & smartphones

Litho opportunity :
- Overlay & LE^2 process control
- Capacity additions

Source: ASML

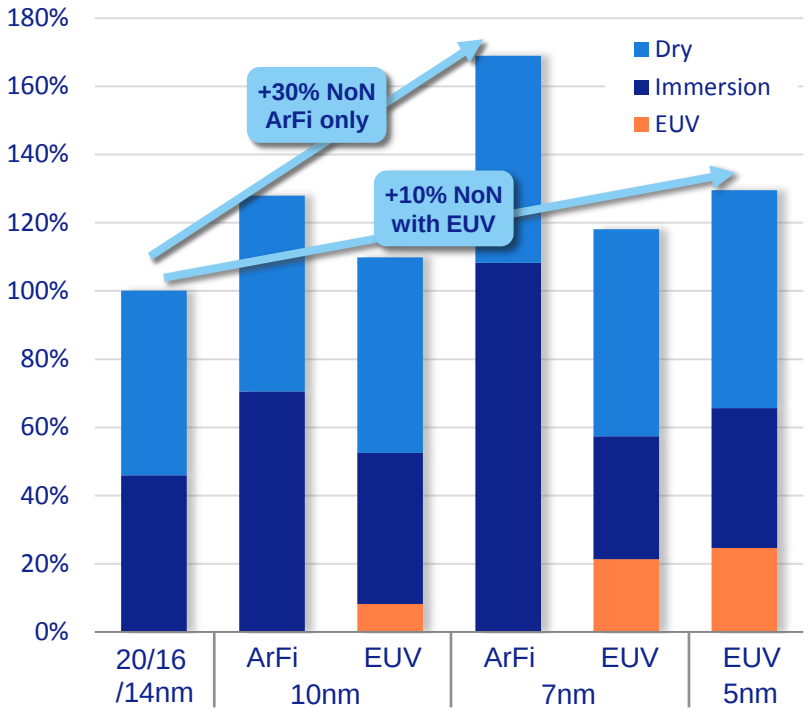
Logic market transitions & ASML opportunities



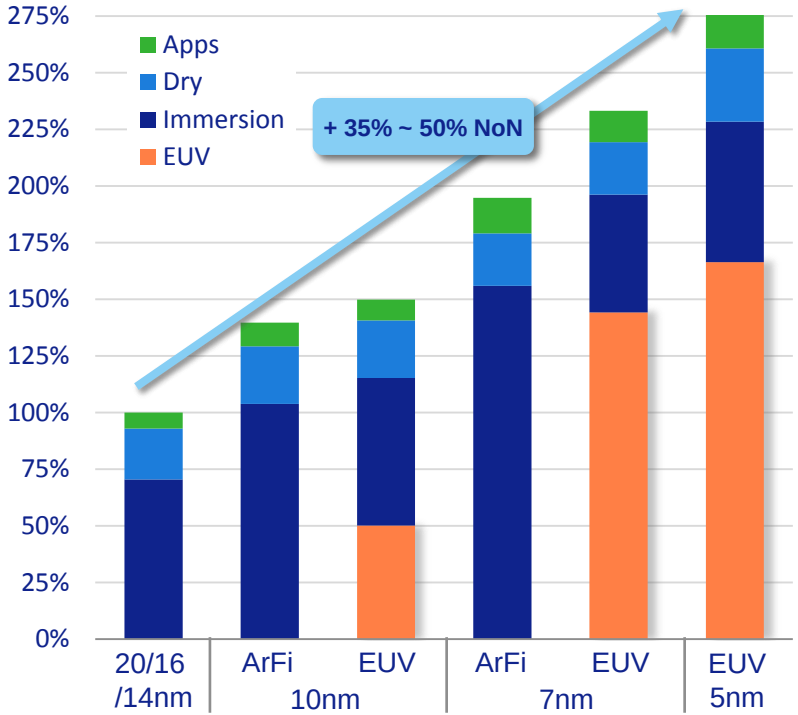
Source: ASML

Logic market opportunity: increased # passes with Multiple-Patterning, higher Litho CapEx with EUV

Relative # Exposure Passes



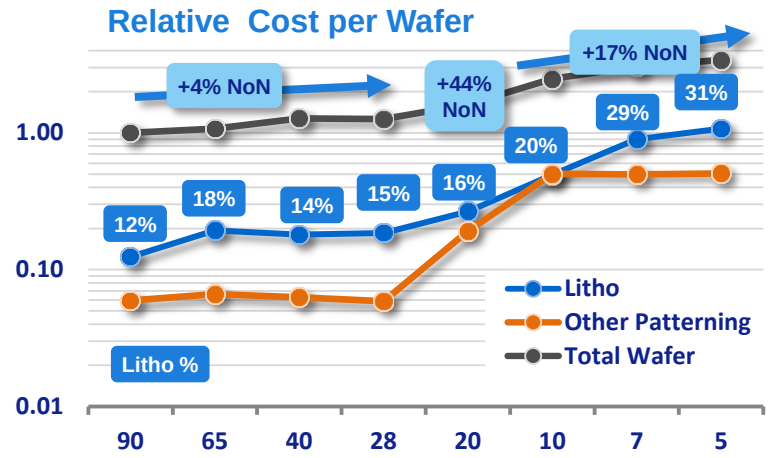
Relative CapEx / 1k WSpM

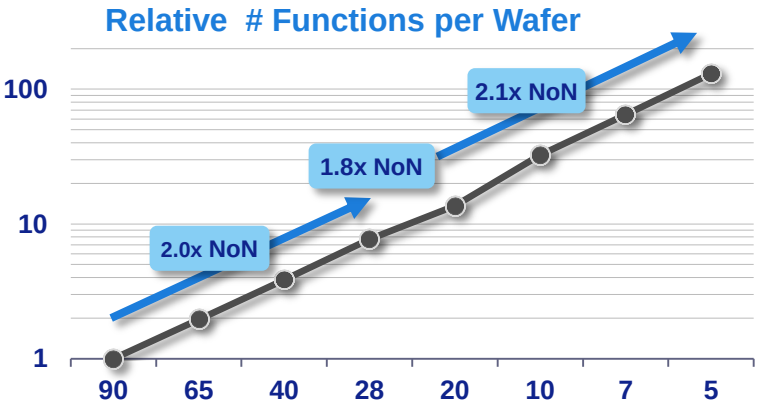


Source: ASML

Logic Cost / Function returns to historical trends with EUV

Litho CapEx share grows as multiple patterning costs reduced





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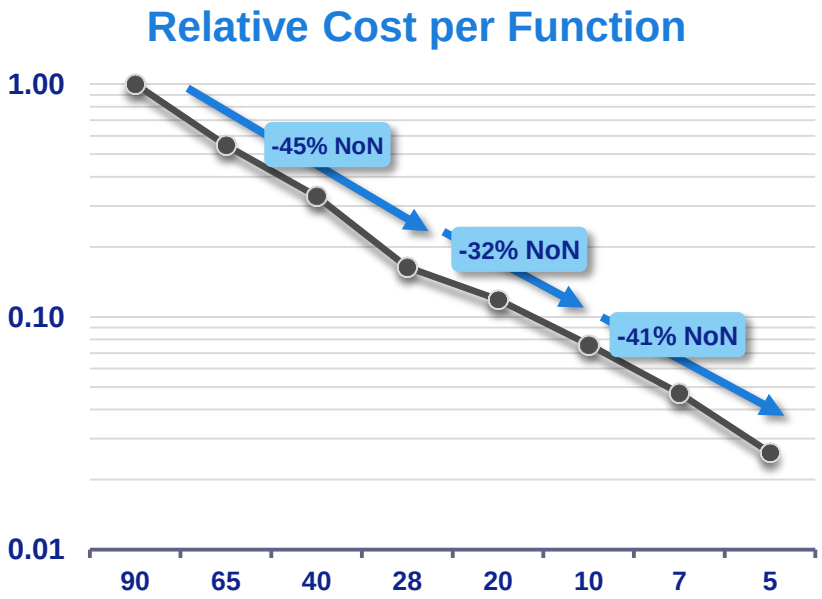


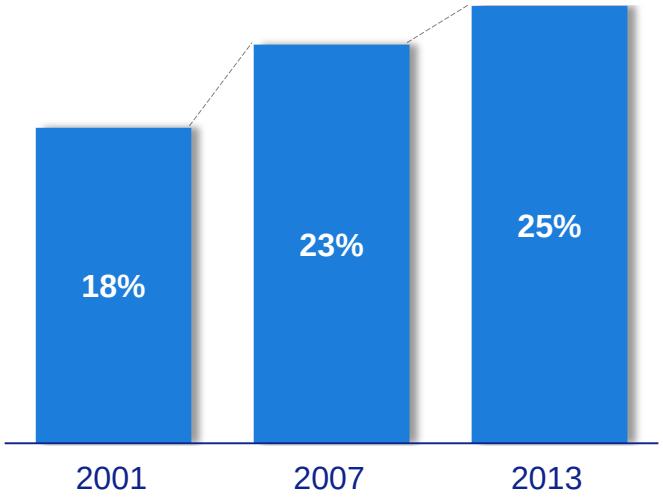
NoN = Node on Node

Source: ASML, IC Knowledge, IMEC
Validated with external consultants

External sources support the continued growth of Litho

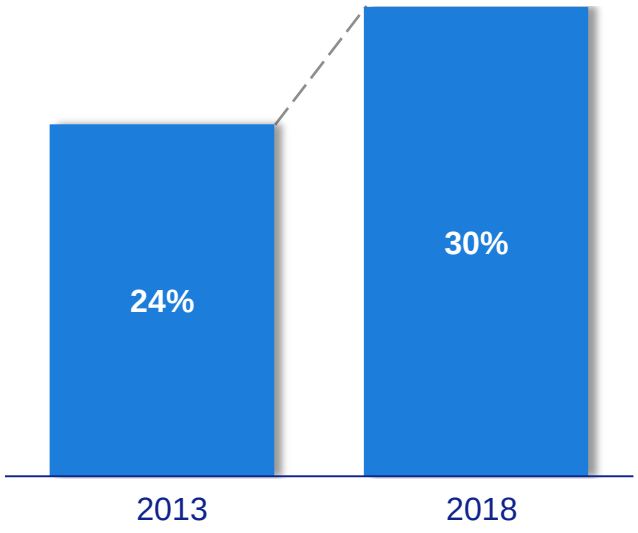
Historically Litho's share of the equipment market has grown

Litho's share of Wafer Equipment, SEMI



Independent research analysts expect Litho's share in equipment to increase

Litho's share of Wafer Equipment spend, Gartner



Summary

- **Moore's law continues**
  - Strong technology pipeline & competition to continue scaling memory & logic
  - Supported by a large profit pool and incentive to make it happen
- **ASML delivers compelling Customer value**
  - EUV - to enable continued cost effective shrink
  - Holistic Litho – to secure high productivity & yield in high volume manufacturing
  - System upgrades – to enable affordable node transitions
- **Resulting in a great market opportunity**
  - Increasing Litho CapEx / wafer at each new node
  - Growing Litho share of total equipment CapEx spend

ASML

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